ABSTRACT

A method for refreshing PCRAM cells programmed to a low resistance state and entire arrays of PCRAM cells uses a simple refresh scheme which does not require separate control and application of discrete refresh voltages to the PCRAM cells in an array. Specifically, the array structure of a PCRAM device is constructed to allow leakage current to flow through each programmed cell in the array to refresh the programmed state. In one embodiment, the leakage current flows across the access device between the anode of the memory element and the bit line to which the cell is connected, for each memory cell in the array which has been programmed to the low resistance state. In another embodiment, the leakage current flows to the programmed cells through a doped substrate or doped regions of a substrate on which each cell is formed. An entire array is refreshed simultaneously by forming each memory element in the array to have one common anode formed as a single cell plate for the array. Only PCRAM cells in the array written to the low resistance state are refreshed by the controlled leakage current, whereas cells in the high resistance state are not affected by the refresh operation.